

Serial No. 09/611,955
Art Unit: 2811

Applicant includes a new Abstract. Applicant proposes the drawing changes set forth in the attached letter to the Official Draftsman. The present invention is directed to the structure embodiment shown in Fig. 3. The entire structure 3, 4, 6, 8 is located in a recess 2 over at least one major surface of the substrate 13.

Applicant believes any objection to the drawing figures is overcome. Examiner's comments 2-6.

35 U.S.C. 112

Applicant incorporates its REMARKS filed on/about October 19, 2001, March 28, 2002 and May 28, 2002, but proposes the drawing figures as now attached in the instant Letter.

Figure 3 shows a recess 2 in at least one major surface of a substrate 13 (space below layer 3), an insulating layer 3 located over the major surface and in the recess 2, a barrier 4 located over layer 3 and in recess 2 and over the major surface, a seed layer 6 located over 4 within the recess 2, and a metal 8 in the recess 2.

Note that Figure 4 does not separately show seed layer 6, which is understood therein to be one with metal 8. Examiner's comment 6.

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35 U.S.C. 102/103

To the extent that any art rejection is applied, reconsideration is requested. Jain neither teaches, discloses nor suggests the structure of thrice amended claim 25 (Fig. 3) of the instant invention.

In Jain, the seed layer 60 is not restricted to a recess, but rather is continuous over the entire Figure 7. Figure 10 of Jain, respectfully, is not germane to Applicant's invention (claim 25, thrice amended).

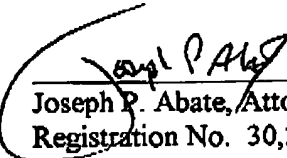
As shown in Fig. 7 of Jain, and contrary to Applicant's invention, the seed layer 60 is not located within a recess only. In addition, Jain fails to teach Applicant's seed layer 6 in combination with the remaining elements of claim 25 (thrice amended), such as a conductive metal 8 in the recess 2 only.

Accordingly, Applicant believes any art rejection is overcome. Examiner's comments 7, 8.

Entry of this Amendment, and allowance of claims 25-32 are solicited.

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE**In the Specification:****Please amend the paragraph beginning at page 7, line 16, as follows:**

-- In accordance with the present invention, recesses 2 such as troughs and vias are provided [on]in at least one major surface of a semiconductor substrate [(not shown)]13. Typical semiconductor substrates include silicon and group III-V semiconductors. Electrical insulation 3 is provided over the major surface and in the recesses such as silicon dioxide which can be thermally grown or deposited such as by chemical vapor deposition or physical vapor deposition. Typically, the insulating layer is about 2000 to about 30,000 Å thick, and more typically about 4000 to about 20,000 Å thick.--

Please amend the paragraph beginning at page 13, line 1, as follows:

-- According to an alternative process according to the present invention, recesses 2 such as troughs and vias are provided [on]in at least one major surface of a semiconductor substrate [(not shown)]13. Electrical insulation 3 is provided over the major surface and in the recesses such as silicon dioxide which can be thermally grown or deposited such as by chemical vapor deposition or physical vapor deposition. Typically, the insulating layer is about 2000 to about 30,000 Å thick, and more typically about 4000 to about 20,000 Å thick.--

FIS919970205US2

December 23, 2002

Application Serial No. 09/611,955**Page 2 of 2****In the Claims:****Kindly amend claims 25, 31 and 32 as follows:**

25. (Thrice Amended) A semiconductor structure, comprising: a semiconductor substrate; a recess[es] located in at least one major surface of said semiconductor substrate; an electrical insulating layer located over said at least one major surface and in said recess[es]; a conductive barrier located over said insulating layer in said recess[es] and over said at least one major surface; a plating seed layer located over said conductive barrier within said recess[es] only; and a conductive metal in said recess[es] only.

31. (Amended) The semiconductor structure of claim 25 wherein said [electroplated] conductive metal is copper.

32. (Amended) The semiconductor structure of claim 31 wherein said [electroplated] conductive metal is about 4000 Å to about 30,000 Å thick.

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